Amendments to the Specification:

On page 8, line 29, please insert the following paragraph before the paragraph beginning with "FIG. 5E is a...":

FIG. 5D-1 is an enlarged view of the encircled portion of FIG. 5D;

On page 11, please amend the paragraph beginning on line 6 and ending on line 9 as follows:

Dotted lines 23 inside the dam bars 17 represent singulation lines along which the lead frame 10' is cut after completing a semiconductor chip mounting process, a wire bonding process, and a resin encapsulate molding process. In Fig. ~~10A~~ **1**, the reference numeral 18 denotes side rails.

On page 14, please amend the paragraph beginning on line 19 and ending on line 25 as follows:

In the case of Fig. 5D, ~~Z-shaped~~ **L-shaped** wings extend from opposite side edges of each inner lead 12 at the inner end of the inner lead 12, respectively. Each wing has a partially etched structure in such a fashion that its lower surface has a higher level than that of the lower surface of the associated inner lead 12 to provide a lead lock 14. **Further, facing L-shaped wings of adjacent leads are oppositely oriented.** No wing is provided at the side edge of each inner lead 12 arranged adjacent to an associated one of the tie bars 15. However, this is not construed to limit the present invention. Also, although the wings have a ~~Z~~ **L** shape, they may have other shapes.

On page 17, please amend the paragraph beginning on line 21 and ending on line 3 of page 18 as follows:

The semiconductor package 1 of Fig. 7C has the same basic configuration as that of Fig. 7A. Accordingly, no description will be made for the same basic configuration. In the case of Fig. 7C, an insulating material such as polyimide is uniformly coated over the entire lower surface of the semiconductor chip 2 using a well-known process such as a spin

coating process, a duct blade process, a spraying process, a dispensing process or a printing process. The coated layer is then set at a high temperature. Practically, the insulating material is coated over a wafer (not shown) including a plurality of semiconductor chips 2. Accordingly, a sawing process is carried out to separate the wafer into package units respectively including individual semiconductor chips 2 each coated with the insulating layer 32 over the entire lower surface thereof. Each semiconductor chip 2 is then mounted on the paddle 16 of a lead frame having a configuration according to the present invention by means of a well-known thermally conductive-adhesive layer **31**. In the case of FIG. 7C, accordingly, the inner end of each lead 11 is maintained not to come into direct contact with the lower surface of the semiconductor chip 2. As a result, there is no problem such as a short circuit or electric leakage even when the semiconductor chip 2 is bonded to the paddle 16 without keeping its accurate horizontal position or when a lead sweeping phenomenon occurs during a molding process.

On page 18, please amend the paragraph beginning on line 28 and ending on line 2 of page 19 as follows:

Fig. 8 is an enlarged view corresponding to a portion A of Fig. 7D. Referring to Fig. 8, a configuration capable of accomplishing the fifth object of the present invention will be described. Fig. 8 illustrates a cross-section of a structure obtained after cleaning the solder ball lands 19a by removing the lower portion of each protrusion 19, exposed at the bottom of the resin encapsulate 4 in the semiconductor package 1, to a desired depth and over a desired area, selectively plating **a metal 35 such as** gold and/or nickel, and/or aluminum, or an alloy thereof on the cleaned solder ball lands 19a and then fusing solder balls 5, as external input/output terminals, on the plated solder ball lands 19a.